

File View Edit Tools Window Help

DB: USPAT;US-PCPUB;EPQ;JPO

Default operator: OR

Highlight all hit terms only

Silicon-on-insulator or SOI and (fully near depleted)

☐ Drafts  
☐ Pending  
☒ Active  
☐ Failed  
☐ Saved  
☐ Favorites  
☐ Tagged (0)  
☐ LDC  
☐ Queue

☐ L1: (0) fully near depleted and silicon  
☐ L2: (0) fully near depleted and silicon  
☐ L3: (3) silicon-on-insulator and substrate  
☐ L4: (0) silicon-on-insulator and substrate  
☐ L5: (8-5) silicon-on-insulator and substrate  
☐ L6: (440) silicon-on-insulator and substrate  
☐ L7: (27) silicon-on-insulator and substrate  
☐ L8: (50) (silicon-on-insulator SOI) and substrate  
☐ L9: (12) (silicon-on-insulator SOI) and substrate  
☐ L10: (3) silicon-on-insulator and substrate  
☐ L11: (0) fully near depleted and silicon  
☐ L12: (91) extractor near contact  
☐ L13: (2) 12 and (silicon-on-insulator SOI)  
☐ L14: (30) extractor and (silicon-on-insulator)  
☐ L15: (521) (silicon-on-insulator or SOI) with  
☐ L16: (1) 15 and (contact with (reverse near bias))  
☐ L18: (4) 17 and ((reverse near bias) with  
☐ L19: (2) 17 and ((reverse near bias) with

☐ (0) 15 and (contact with (reverse near bias))

	U	I	Document ID	Issue Date	Pages	Title	Current GR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20040126969 A1	20040701	13	DRAM cell with enhanced SER immunity	438/257	
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040124490 A1	20040701	8	Local isolation for fully-depleted SOI devices	257/506	
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040124488 A1	20040701	30	Semiconductor device	257/437	
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040124470 A1	20040701	9	Wafer Bonding Method Of Forming Silicon-On-Insulator Comprising Integrated	257/347	
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040121605 A1	20040624	36	Method and apparatus to improve thickness uniformity of surfaces for	438/694	
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040121596 A1	20040624	36	Method and apparatus for planarization of a material by growing a sacrificial film with	438/689	
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040121507 A1	20040624	37	Semiconductor devices with reduced active region defects and unique contacting	438/93	257/431; 257/616;
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040119136 A1	20040624	17	BIPOLEAR TRANSISTOR HAVING A MAJORITY-CARRIER ACCUMULATION	257/526	257/517; 257/518;
9	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040113210 A1	20040617	9	Novel field effect transistor and method of fabrication	257/401	257/188; 257/333;
10	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040113207 A1	20040617	24	Vertical MOSFET SRAM cell	257/368	257/379; 257/393;
11	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040108552 A1	20040610	14	Semiconductor device with SOI region and bulk region and method of manufacture	257/347	

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